

Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. **(Currently Amendment)** A liquid crystal display device having a plurality of pixels, each of the plurality of pixels comprising:

- a plurality of memory circuits;
- a plurality of non-volatile memory circuits;
- a plurality of first switches, wherein each of the plurality of first switches is electrically connected to a corresponding one of the plurality of memory circuits;
- a plurality of second switches, wherein each of the plurality of second switches is electrically connected to a corresponding one of the plurality of non-volatile memory circuits;
- a plurality of third switches, wherein each of the plurality of third switches is electrically connected to a corresponding one of the plurality of memory circuits;
- a plurality of fourth switches, wherein each of the plurality of fourth switches is electrically connected to a corresponding one of the plurality of non-volatile memory circuits;
- a plurality of read transistors, wherein each of the plurality of read transistors is electrically connected to a corresponding one of the plurality of first switches, and to a corresponding one of the plurality of second switches;
- a plurality of write transistors, wherein each of the plurality of write transistors is electrically connected to a corresponding one of the plurality of third switches, and to a corresponding one of the plurality of the fourth switches; and
- a liquid crystal element electrically connected to each one of the plurality of **[[write]]** read transistors.

2. (Original) A device according to claim 1, wherein the memory circuits are static random access memories (SRAM).

3. (Original) A device according to claim 1, wherein the memory circuits are ferroelectric random access memories (FeRAM).

4. (Original) A device according to claim 1, wherein the memory circuits are dynamic random access memories (DRAM).

5. (Original) A device according to claim 1, wherein the non-volatile memory circuits are non-volatile electrically erasable programmable read only memories (EEPROM).

6. (Original) A device according to claim 1, wherein the memory circuits are formed on a glass substrate.

7. (Original) A device according to claim 1, wherein the memory circuits are formed on a plastic substrate.

8. (Original) A device according to claim 1, wherein the memory circuits are formed on a stainless steel substrate.

9. (Original) A device according to claim 1, wherein the memory circuits are formed on a single crystal wafer.

10. (Previously Presented) An device according to claim 1, wherein the liquid crystal display device is incorporated in an electronic device.

11. (Original) An device according to claim 10, wherein the electronic device is selected from the group consisting of a television set, a personal computer, a portable terminal, a video camera, and a head mounted display.

12. **(Currently Amendment)** A liquid crystal display device having a plurality of pixels, each of the plurality of pixels comprising:

$n \times m$ memory circuits for storing m (m is a natural number and satisfies $1 \leq m$) frames of n (n is a natural number and satisfies $2 \leq n$) bit digital video signals;

$n \times k$ non-volatile memory circuits for storing k (k is a natural number and satisfies $1 \leq k$) frame of the n bit digital video signals;

n first switches, wherein each of the n first switches is electrically connected to a corresponding one of the $n \times m$ memory circuits;

n second switches, wherein each of the n second switches is electrically connected to a corresponding one of the $n \times k$ non-volatile memory circuits;

n third switches, wherein each of the n third switches is electrically connected to a corresponding one of the $n \times m$ memory circuits;

n fourth switches, wherein each of the n fourth switches is electrically connected to a corresponding one of the $n \times k$ non-volatile memory circuits;

n read transistors, wherein each of the n read transistors is electrically connected to a corresponding one of the n first switches, and to a corresponding one of the n second switches;

n write transistors, wherein each of the n write transistors is electrically connected to a corresponding one of the n third switches, and to a corresponding one of the n fourth switches; and

a liquid crystal element electrically connected to each one of the n ~~[[write]]~~ read transistors.

13. (Original) A device according to claim 12, wherein the memory circuits are static random access memories (SRAM).

14. (Original) A device according to claim 12, wherein the memory circuits are ferroelectric random access memories (FeRAM).

15. (Original) A device according to claim 12, wherein the memory circuits are dynamic random access memories (DRAM).

16. (Original) A device according to claim 12, wherein the non-volatile memory circuits are non-volatile electrically erasable programmable read only memories (EEPROM).

17. (Original) A device according to claim 12, wherein the memory circuits are formed on a glass substrate.

18. (Original) A device according to claim 12, wherein the memory circuits are formed on a plastic substrate.

19. (Original) A device according to claim 12, wherein the memory circuits are formed on a stainless steel substrate.

20. (Original) A device according to claim 12, wherein the memory circuits are formed on a single crystal wafer.

21. (Previously Presented) An device according to claim 12, wherein the liquid crystal display device is incorporated in an electronic device.

22. (Previously Presented) An device according to claim 21, wherein the electronic device is selected from the group consisting of a television set, a personal computer, a portable terminal, a video camera, and a head mounted display.

23. (Original) A liquid crystal display device having a plurality of pixels, each of the plural pixels comprising:

a source signal line;

n (n is a natural number and satisfies $2 \leq n$) writing gate signal lines;

n reading gate signal lines;

n writing transistors;

n reading transistors;

$n \times m$ memory circuits for storing m (m is a natural number and satisfies $1 \leq m$) frames of n bit digital video signals;

$n \times k$ non-volatile memory circuits for storing k (k is a natural number and satisfies $1 \leq k$) of the n bit digital video signals;

$2n$ memory circuit selecting units;

$2n$ non-volatile memory circuit selecting units; and

a liquid crystal element,

wherein each gate electrode of the n writing transistors is electrically connected to one of the n writing gate signal lines, with no two gate electrodes sharing the same writing gate signal line,

wherein each input electrode of the n writing transistors is electrically connected to the source signal line,

wherein each output electrode of the n writing transistors is electrically connected to one of m circuits out of the $n \times m$ memory circuits through one of n units out of the $2n$ memory circuit selecting units, each memory circuit selecting unit making selection for no more than one output electrode,

wherein each output electrode of the n writing transistors is electrically connected to one of k circuits out of the $n \times k$ non-volatile memory circuits through one of n units out of the $2n$ non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one output electrode,

wherein each gate electrode of the n reading transistors is electrically connected to one of the n reading gate signal lines, with no two gate electrodes sharing the same reading gate signal line,

wherein each input electrode of the n reading transistors is electrically connected to one of m circuits out of the $n \times m$ memory circuits through one of n units out of the $2n$ memory circuit selecting units, each memory circuit selecting unit making selection for no more than one input electrode,

wherein each input electrode of the n reading transistors is electrically connected to one of k circuits out of the $n \times k$ non-volatile memory circuits through one of n units of the $2n$ non-

volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one input electrode, and

wherein each output electrode of the n reading transistors is electrically connected to one of electrodes of the liquid crystal element.

24. (Original) A device according to claim 23,

wherein one of the m memory circuits is selected by one of the memory circuit selecting units, or one of the k non-volatile memory circuits is selected by one of the non-volatile memory circuit selecting unit, to communicate the selected memory circuit or non-volatile memory circuit with the output electrode of its associated writing transistor, thereby writing the digital video signals in the selected memory circuit, or

wherein one of the m memory circuits is selected by one of the memory circuit selecting units, or one of the k non-volatile memory circuits is selected by one of the non-volatile memory circuit selecting unit, to communicate the selected memory circuit or non-volatile memory circuit with the input electrode of its associated reading transistor, thereby reading the digital video signals stored in the selected memory circuit.

25. (Original) A device according to claim 23, further comprising:

shift registers for outputting sampling pulses sequentially in response to clock signals and start pulses;

first latch circuits for holding n (n is a natural number and satisfies $2 \leq n$) bit digital video signals in response to the sampling pulses;

second latch circuits for receiving the n bit digital video signals that have been held in the first latch circuits; and

bit selecting circuits for selecting the n bit digital video signals transferred to the second latch circuits one bit by one bit to output the signals to the source signal line.

26. (Original) A device according to claim 23, wherein the memory circuits are static random access memories (SRAM).

27. (Original) A device according to claim 23, wherein the memory circuits are ferroelectric random access memories (FeRAM).

28. (Original) A device according to claim 23, wherein the memory circuits are dynamic random access memories (DRAM).

29. (Original) A device according to claim 23, wherein the non-volatile memory circuits are non-volatile electrically erasable programmable read only memories (EEPROM).

30. (Original) A device according to claim 23, wherein the memory circuits are formed on a glass substrate.

31. (Original) A device according to claim 23, wherein the memory circuits are formed on a plastic substrate.

32. (Original) A device according to claim 23, wherein the memory circuits are formed on a stainless steel substrate.

33. (Original) A device according to claim 23, wherein the memory circuits are formed on a single crystal wafer.

34. (Previously Presented) An device according to claim 23, wherein the liquid crystal display device is incorporated in an electronic device.

35. (Previously Presented) An device according to claim 34, wherein the electronic device is selected from the group consisting of a television set, a personal computer, a portable terminal, a video camera, and a head mounted display.

36. (Original) A liquid crystal display device having a plurality of pixels, each of the plural pixels comprising:

n (n is a natural number and satisfies $2 \leq n$) source signal lines;
a writing gate signal line;
n reading gate signal lines;
n writing transistors;
n reading transistors;
n x m memory circuits for storing m (m is a natural number and satisfies $1 \leq m$) frames of
n bit digital video signals;
n x k non-volatile memory circuits for storing k (k is a natural number and satisfies $1 \leq k$)
of the n bit digital video signals;
2n memory circuit selecting units;
2n non-volatile memory circuit selecting units; and
a liquid crystal element,
wherein each gate electrode of the n writing transistors is electrically connected to the
writing gate signal line,
wherein each input electrode of the n writing transistors is electrically connected to one
of the n source signal lines, with no two input electrodes sharing the same source signal line,
wherein each output electrode of the n writing transistors is electrically connected to one
of m circuits out of the n x m memory circuits through one of n units out of the 2n memory
circuit selecting units, each memory circuit selecting unit making selection for no more than one
output electrode,
wherein each output electrode of the n writing transistors is electrically connected to one
of k circuits out of the n x k non-volatile memory circuits through one of n units out of the 2n
non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit
making selection for no more than one output electrode,
wherein each gate electrode of the n reading transistors is electrically connected to one of
the n reading gate signal lines, with no two gate electrodes sharing the same reading gate signal
line,
wherein each input electrode of the n reading transistors is electrically connected to one
of m circuits out of the n x m memory circuits through one of n units out of the 2n memory

circuit selecting units, each memory circuit selecting unit making selection for no more than one input electrode,

wherein each input electrode of the n reading transistors is electrically connected to one of k circuits out of the $n \times k$ non-volatile memory circuits through one of n units out of the $2n$ non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one input electrode, and

wherein each output electrode of the n reading transistors is electrically connected to one of electrodes of the liquid crystal element.

37. (Original) A device according to claim 36,

wherein one of the m memory circuits is selected by one of the memory circuit selecting units, or one of the k non-volatile memory circuits is selected by one of the non-volatile memory circuit selecting unit, to communicate the selected memory circuit or non-volatile memory circuit with the output electrode of its associated writing transistor, thereby writing the digital video signals in the selected memory circuit, or

wherein one of the m memory circuits is selected by one of the memory circuit selecting units, or one of the k non-volatile memory circuits is selected by one of the non-volatile memory circuit selecting unit, to communicate the selected memory circuit or non-volatile memory circuit with the input electrode of its associated reading transistor, thereby reading the digital video signals stored in the selected memory circuit.

38. (Original) A device according to claim 36, further comprising:

shift registers for outputting sampling pulses sequentially in response to clock signals and start pulses;

first latch circuits for holding 1 bit digital video signal out of n (n is a natural number and satisfies $2 \leq n$) bit digital video signals in response to the sampling pulses; and

second latch circuits for receiving the 1 bit digital video signal that has been held in the first latch circuits to output the 1 bit digital video signal to the source signal lines.

39. (Original) A device according to claim 36, further comprising:

shift registers for outputting sampling pulses sequentially in response to clock signals and start pulses;

latch circuits for holding 1 bit digital video signal in response to the sampling pulses; and
bit selecting circuits for selecting one of the source signal lines in order to output the 1 bit digital video signal that has been held in the latch circuits to the selected source signal line.

40. (Original) A device according to claim 36, wherein the memory circuits are static random access memories (SRAM).

41. (Original) A device according to claim 36, wherein the memory circuits are ferroelectric random access memories (FeRAM).

42. (Original) A device according to claim 36, wherein the memory circuits are dynamic random access memories (DRAM).

43. (Original) A device according to claim 36, wherein the non-volatile memory circuits are non-volatile electrically erasable programmable read only memories (EEPROM).

44. (Original) A device according to claim 36, wherein the memory circuits are formed on a glass substrate.

45. (Original) A device according to claim 36, wherein the memory circuits are formed on a plastic substrate.

46. (Original) A device according to claim 36, wherein the memory circuits are formed on a stainless steel substrate.

47. (Original) A device according to claim 36, wherein the memory circuits are formed on a single crystal wafer.

48. (Previously Presented) A method according to claim 36, further comprising incorporating the liquid crystal display device in an electronic device.

49. (Original) A method according to claim 48, wherein the electronic device is selected from the group consisting of a television set, a personal computer, a portable terminal, a video camera, and a head mounted display.

50. (Previously Presented) A method of driving a liquid crystal display device using n (n is a natural number and satisfies $2 \leq n$) bit digital video signals to display an image, the liquid crystal display device including a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels,

wherein shift registers in the source signal line driver circuit output sampling pulses, which are inputted to latch circuits, which hold the digital video signals in response to the sampling pulses, the held digital video signals being written in a source signal line,

wherein gate signal line selecting pulses are outputted in the gate signal line driver circuit to select a gate signal line, and

wherein one of the following (a) through (e) is selected and conducted in pixels in the row of the selected gate signal line out of the plural pixels:

(a) the n bit digital video signals inputted from the source signal line are written in memory circuits;

(b) the n bit digital video signals stored in the memory circuits are read;

(c) the n bit digital video signals inputted from the source signal line or the n bit digital video signals stored in the memory circuits are written in non-volatile memory circuits;

(d) the n bit digital video signals stored in the non-volatile memory circuits are read; and

(e) the n bit digital video signals stored in the non-volatile memory circuits are written in the memory circuits.

51. (Previously Presented) A method according to claim 50, wherein, during a still image display period, the n bit digital video signals stored in the non-volatile memory circuits are

repeatedly read to display a still image, so that the source signal line driver circuit can stop its operation.

52. (Previously Presented) A method according to claim 50, further comprising incorporating the liquid crystal display device in an electronic device.

53. (Previously Presented) A method to claim 52, wherein the electronic device is selected from the group consisting of a television set, a personal computer, a portable terminal, a video camera, and a head mounted display.

54. (Withdrawn) A method of driving a liquid crystal display device using n (n is a natural number and satisfies $2 \leq n$) bit digital video signals to display an image, the liquid crystal display device including a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels, wherein shift registers in the source signal line driver circuit output sampling pulses, which are inputted to latch circuits, which hold the digital video signals in response to the sampling pulses, the held digital video signals being written in a source signal line, wherein gate signal line selecting pulses are outputted in the gate signal line driver circuit to select gate signal lines in order from the first row, and wherein the n bit digital video signals are written in or read out the plural pixels in order from the first row.

55. (Withdrawn) A method according to claim 54, wherein, during a still image display period, the n bit digital video signals stored in the memory circuits are repeatedly read to display a still image, so that the source signal line driver circuit can stop its operation.

56. (Withdrawn) A method according to claim 54, further comprising incorporating the liquid crystal display device in an electronic device.

57. (Withdrawn) A method according to claim 56, wherein the electronic device is selected from the group consisting of a television set, a personal computer, a portable terminal, a

video camera, and a head mounted display.

58. (Withdrawn) A method of driving a liquid crystal display device using n (n is a natural number and satisfies $2 < n$) bit digital video signals to display an image, the liquid crystal display device including a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels, wherein shift registers in the source signal line driver circuit output sampling pulses, which are inputted to latch circuits, which hold the digital video signals in response to the sampling pulses, the held digital video signals being written in a source signal line, wherein the gate signal line driver circuit selects a gate signal line by outputting a gate signal line selecting pulse to an arbitrarily specified row of gate signal line, and wherein the n bit digital video signals are written in or read out pixels in the arbitrarily selected row of gate signal line out of the plural pixels.

59. (Withdrawn) A method according to claim 58, wherein, during a still image display period, the n bit digital video signals stored in the memory circuits are repeatedly read to display a still image, so that the source signal line driver circuit can stop its operation.

60. (Withdrawn) A method according to claim 58, further comprising incorporating the liquid crystal display device in an electronic device.

61. (Withdrawn) A method according to claim 60, wherein the electronic device is selected from the group consisting of a television set, a personal computer, a portable terminal, a video camera, and a head mounted display.

62. **(Currently Amended)** A liquid crystal display device having a pixel having:
a liquid crystal element; and
a plurality of sub-pixels, each of the plurality of sub-pixels comprising:
a memory circuit;
a non-volatile memory circuit;
a first switch electrically connected to the memory circuit;

a second switch electrically connected to the non-volatile memory circuit;
a third switch electrically connected to the memory circuit;
a fourth switch electrically connected to the non-volatile memory circuit,
a **[[read]]** write transistor electrically connected to the first switch and to the
second switch; and
a **[[write]]** read transistor electrically connected to the third switch, to the fourth
switch, and to the liquid crystal element.